Digital Step Attenuator

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A 50-ohm digital step attenuator has been developed having 0.2-dB resolution and 51-dB maximum loss. This device has been tested from dc to 10 MHz, where a ±5-degree maximum differential phase shift was measured. Preliminary tests indicate that the attenuator may operate satisfactorily at frequencies as high as 100 MHz. No signal discontinuity occurs during switching, and positive confirmation of step activation is provided. The attenuator is constructed on a 14.5 by 3.2-cm (5.7 by 1.25-in.) double-sided etched circuit card, and occupies a volume of less than 74 cm³ (4.5 in.³).

A computer-controllable attenuator was required to control the 10-MHz input signal level to the Mark III Ranging Demodulator Assembly (RDA). The requirements called for 8-bit resolution (one part in 256) and a total available 51-dB attenuation range. This yields a least-significant-bit (LSB) weight of 0.2 dB. The attenuator was required to have a 50-ohm characteristic impedance, unbalanced to ground. The computer-controllable requirement also made positive confirmation of step actuation mandatory. Since the RDA is a phase-sensitive demodulation system, the attenuator is called upon to maintain less than ±5 degrees differential phase shift over the 51-dB dynamic range at 10 MHz. It was also desirable to insure that no signal discontinuity occurred during step actuation.

The attenuator design was to be as general purpose as possible, and so can accept input from dc to 10 MHz. Solid-state switching of the attenuator steps was ruled out because of the dc response requirement, and because of the difficulty in isolating the signal from the digital controls and noise which might be superimposed upon them. The switching speed of electromechanical relays is entirely adequate for the application, and the low contact resistance yields a lower pad-out insertion loss at the 50-ohm impedance level than can be achieved with solid-state switches.

The digitally controlled step attenuator takes the form of a multiplying digital-to-analog converter (MDAC); that is, the output signal is the product of the input reference

signal and the binary control word. As such, severe constraints are imposed if the device is to maintain monotonicity at both dc and 10 MHz. Resistors employed in the attenuator pads are of the metal film type, possessing low-temperature coefficient (±5 ppm), having low reactance and small skin-effect factor so that the ratio of dc to RF resistance will be low.

To maintain an overall linearity and accuracy of one-half least-significant bit (½ LSB), a ±0.01-dB, dc accuracy per step was imposed. Although ±5% resistor tolerance would satisfy the ±0.01-dB accuracy requirement for the 0.2-dB step, all ±1.0% resistors were utilized in the 0.2 through 3.2-dB steps, ±0.5% for the 6.4-dB stages, and 0.1% for the three 8.533-dB stages (of the 25.6-dB step). Thus, the worst-case tolerance for the eight steps would be ±0.08 dB, which is less than ½ LSB.

The Pi-pad configuration was chosen over the Tee because of a much greater ease of mechanical layout.

Figures 1 and 2 show conventional switching schemes for Pi and Tee pads, respectively. Both require an additional switch pole for confirmation indication, and both open the signal path during switch time-of-flight. Although this latter limitation could be removed by using shorting-type contacts, this is difficult, at best, to achieve with relays.

A slight re-configuring of the Pi-pad as shown in Fig. 3 will remove the signal-loss limitation without the need for shorting-type contacts. Due to switch-lead inductance, the pad-out phase delay will be greater through the short than through the pad for Figs. 1, 2, and 3. This is reduced somewhat in Fig. 3 by the shunting effect of the pad series element. Note in all three of these schemes that, during pad-out conditions, the signal must pass through two contact resistances in series, which for networks at the 50-ohm impedance level will introduce a pad-out insertion loss of approximately 0.035 dB, assuming 100 milliohm contact resistances.

Figure 4 shows a switched Tee-pad arranged to gain the advantages that were gained for the Pi-pad by going from Fig. 1 to Fig. 3. Additionally, Fig. 4 has only one contact resistance in series with the signal during pad-out conditions, thus halving the insertion loss to 0.017 dB.

Since a double-pole double-throw relay is utilized for switching, the circuit of Fig. 4 halves the lead inductance in series with the signal during pad-out condition, thus reducing the differential delay when the pad is switched in. Of the two contacts which have become available, one can now be used as a confirmation indicator. This contact loses ground when the pad is *in*, shown CON "not" (the complement of CONfirmation). This signal can be inverted, if necessary, by utilizing a suitable pull-up resistor.

If a Pi-pad is introduced into the circuit of Fig. 4, all the previous advantages are retained, and a new one added. The Pi-pad resistors physically group around the relay in a two-dimensional circuit plane, rather than the three dimensions required for the Tee.

Referring to Fig. 5, the intrinsic phase delay for the pad-in condition is greater (that is, more negative) than the pad-out delay, for pad attenuation values less than approximately 11.7 dB. These intrinsic delays will add algebraically when considering an assembly of cascaded attenuation stages. Stages having a design loss greater than 11.7 dB will have less (that is, more positive) phase shift. These intrinsic delays will *not* sum algebraically, and can exhibit a composite differential phase shift many times worse than the sum of the individual delays in a multistage assembly.

It was shown that the phase delay of each pad less than 11.7 dB could be reduced to zero by capacitive compensation of the *series* resistive element of the Pi-pads. Similarly, the phase advance of the pads larger than 11.7 dB could be reduced to zero by capacitive compensation of the *shunt* resistive elements of the Pi-pads. However, the *residual* phase shifts for these compensated larger Pi-pads would not sum algebraically. To overcome this problem, the larger attenuation steps were broken into smaller stages such that no individual stage exceeded 11.7 dB.

A residual differential phase shift of ±0.5-degree maximum per stage was realized by use of ±5% tolerance, ±5% incremental-value fixed capacitors. Thus, the need to employ variable trimmer capacitors to achieve the ideal zero residual was avoided.

Figure 6 shows the resultant compensated stage design which is typical of the eleven cascaded stages. Six individual stages are for the 0.2-, 0.4-, 0.8-, 1.6-, 3.2-, and 6.4-dB steps. The 12.8-dB step consists of two 6.4-dB stages, while the 25.6-dB step is composed of three 8.533-dB stages.

The confirmation signals of the individual stages of the 12.8- and 25.6-dB steps are serially ANDed on a separate logic board so as to provide only one confirmation terminal each, for those steps. The serial ANDing provides an additional benefit in that large output signal

excursions will not occur during the switching time for the two largest steps. This feature, coupled with the no-signal-loss switching scheme, limits the level excursion to less than one-third of the most-significant bit, i.e., less than 8.533 dB.

Figure 7 shows the functional layout of the stages, which are arranged on a double-sided etched circuit board 3.2 cm (1.25 inches) wide by 14.5 cm (5.7 inches) long. Each stage is in a keystone-shaped modular form so as to group alternately in a space-conserving fashion, and to minimize interstage conductor length. The end areas are for connector termination. The signal travels down the long center axis of the board, and signal-carrying conductors assume strip-line dimensions where practical, to minimize VSWR. The complete attenuator occupies a volume of less than 74 cm^3 (4.5 $in.^3$).

This device has been tested from dc to 10 MHz, where a $\pm$5-degree maximum phase shift was measured. Preliminary data indicate that the attenuator may perform satisfactorily at frequencies up to 100 MHz.

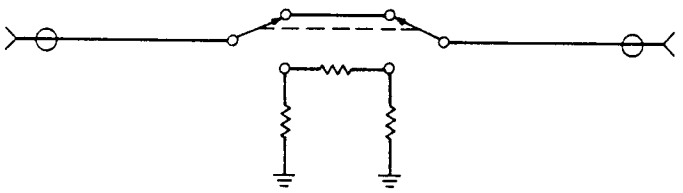

Fig. 1. Pi configuration

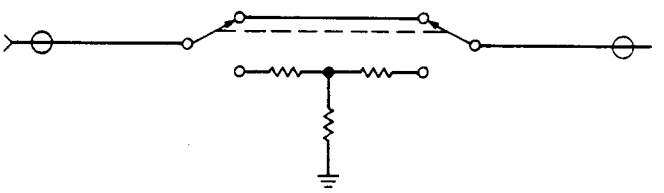

Fig. 2. Tee configuration

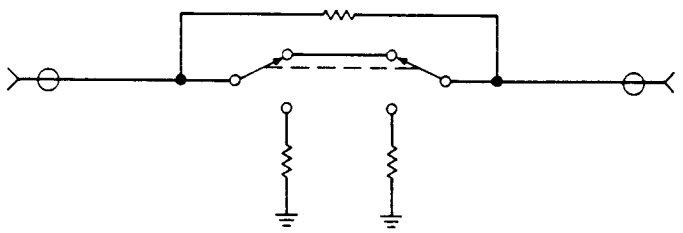

Fig. 3. Modified Pi

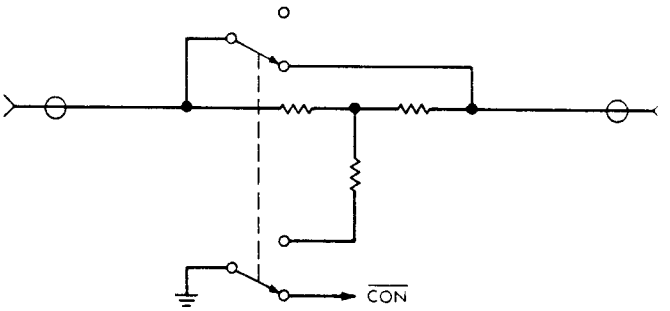

Fig. 4. Tee with confirmation

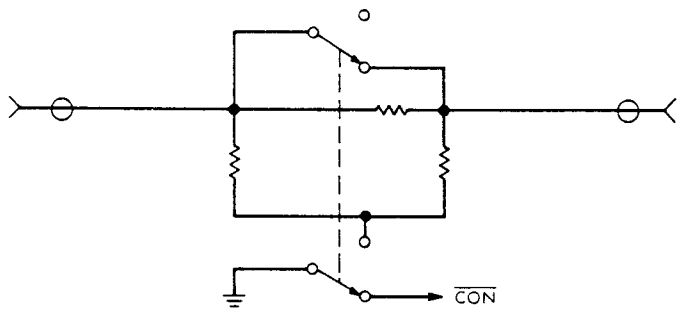

Fig. 5. Pi with confirmation

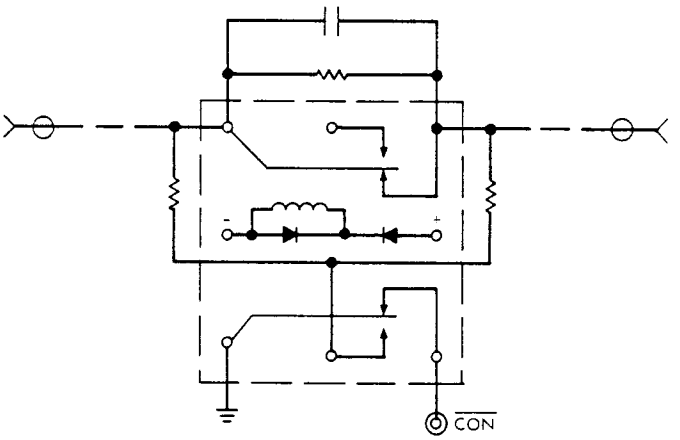

Fig. 6. Compensated Pi with confirmation

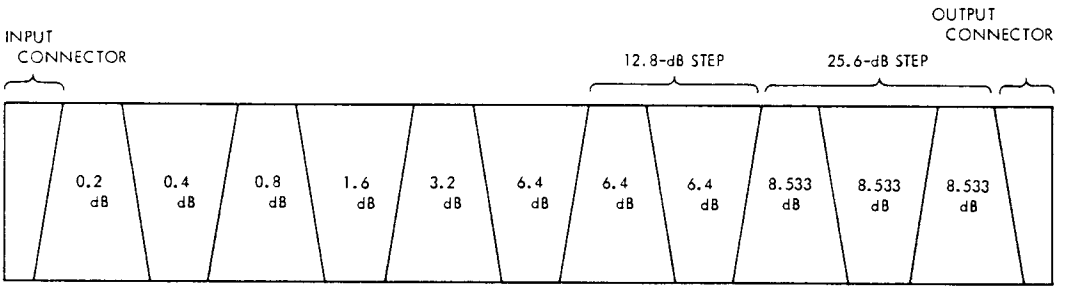

Fig. 7. Functional layout of stages